AMENDMENTS

In the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. – 13. (Canceled)

14. (Currently amended) A flash memory device comprising:

a substrate;

a stacked gate comprising a floating gate and a control gate wherein said floating gate comprises a first oxide layer overlying said substrate and a floating gate layer overlying said first oxide layer and wherein said control gate comprises a second oxide layer overlying said floating gate layer and a control gate layer overlying said second oxide layer;

source and drain regions in said substrate adjacent to said stacked gate;

a third oxide layer on the sidewalls of said stacked gate; and

a conductive plugs contacting said source and drain regions wherein said conductive plugs extend parallel to said stacked gate and wherein said conductive plug layer provides coupling of between said drain and source and said floating gate,

wherein the surface area between the conductive plug and the floating gate is larger than the overlap surface between the floating gate and said source and drain regions.

15. (Original) The device according to claim 14 wherein said floating gate layer comprises polysilicon.

16. (Original) The device according to claim 14 wherein said control gate layer comprises polysilicon.

17. (Original) The device according to claim 14 wherein said conductive plugs comprises polysilicon.

18. (Original) The device according to claim 14 wherein the surface profile of said floating gate layer is angled to enhance an electric field.

19. (Original) The device according to claim 14 wherein adjacent stacked gates are separated by STI regions that protrude substantially above said substrate.

20. (Original) The device according to claim 14 further comprising: a masking layer overlying said conductive plug coupled to said source;

a patterned bit line layer overlying said conductive plug coupled to said drain, said masking layer, and said stacked gates.

21. (Original) The device according to claim 20 wherein said patterned bit line layer comprises polysilicon.

22. (Original) The device according to claim 14 wherein said floating gate is programmed by forcing a negative voltage across said control gate and said source and drain conductive plugs.

23. (Original) The device according to claim 14 wherein said floating gate is erased by forcing a positive voltage across said control gate and said source and drain conductive plugs.

24. (Original) The device according to claim 14 wherein said floating gate is erased by forcing a first positive voltage across said control gate and said source conductive plug and a second, smaller positive voltage across said control gate and said drain conductive plug.

25. (Original) The device according to claim 14 wherein said floating gate is read by forcing a first positive voltage across said control gate and said source conductive plug and a second, smaller positive voltage across said control gate and said drain conductive plug.

26. (New) A flash memory device comprising:

a substrate;

a stacked gate comprising a floating gate and a control gate wherein said floating gate comprises a first oxide layer overlying said substrate and a floating gate layer overlying said first oxide layer and wherein said control gate comprises a second oxide layer overlying said floating gate layer and a control gate layer overlying said second oxide layer, the surface profile of said floating gate layer is angled to enhance an electric field;

source and drain regions in said substrate adjacent to said stacked gate;

a third oxide layer on the sidewalls of said stacked gate; and conductive plugs contacting said source and drain regions wherein said conductive plugs extend parallel to said stacked gate and wherein said conductive plugs coupling between said drain and source and said floating gate.

27. (New) A flash memory device comprising:

a substrate;

a stacked gate comprising a floating gate and a control gate wherein said floating gate comprises a first oxide layer overlying said substrate and a floating gate layer overlying said first oxide layer and wherein said control gate comprises a second oxide layer overlying said floating gate layer and a control gate layer overlying said second oxide layer;

source and drain regions in said substrate adjacent to said stacked gate;

a third oxide layer on the sidewalls of said stacked gate; and

conductive plugs contacting said source and drain regions wherein said conductive plugs extend parallel to said stacked gate and wherein said conductive plugs provide coupling between said drain and source and said floating gate, wherein adjacent stacked gates are separated by STI regions that protrude substantially above said substrate.